

**Application Number** 09/854,146 Substitute for form 1449A/PTO **Filing Date** 05/11/2001 FORMATION DISCLOSURE **First Named Inventor** Jun Li TATEMENT BY APPLICANT Group Art Unit 2812 (use as many sheets as necessary) **Examiner Name** 1 Sheet 1 of Attorney Docket Number SPLX.P0050

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No.1	Number Kin	cument d Code <sup>2</sup> f known)	Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
1/5	1.	5,675,502		Cox	10-07-1997	Abstract, Figs 2, 4 Col. 4-7.
15	2.	5,841,672		Spyrou et al.	11-24-1998	Abstract, Figs 1-3, Col 1-8

FOREIGN PATENT DOCUMENTS							
Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent D	Occument Kind Code (if known) <sup>5</sup>	Name of Patentee or Applicant of Cited Document	Date of Publication MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner* Initials	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>		
VS	3.	SHEPARD, KL: "Practical Issues of Interconnect Analysis in Deep Submicron Integrated Circuits", Proceeding International Conference on Computer Design VLSI in Computers and Processors, Austin, TX, 12-15 Oct. 1997pages 532-541			
<b>V</b> >	4.	KAHNG A B et al.: "Efficient gate Delay Modeling for Large Interconnect Loads", Multi-Chip Module Conference, 1996, MCMC-96, Proceedings, 1996 IEEE Santa Cruz, CA, 6-7, Feb. 1996, pages 202-207			

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